REMARKS

Claims 1-2, 6, 9, 17-18, 22, 25, 33-34, 38, 41 and 49-50 have been amended. Claims 3-5, 7-8, 10-16, 19-21, 23-24, 26-32, 35-37, 39-40, 42-48 and 51-53 have been canceled. Claims 1-2, 6, 9, 17-18, 22, 25, 33-34, 38, 41 and 49-50 remain pending in the present application. Applicant reserves the right to pursue the original claims and other claims in this and other applications.

Claims 1-3, 6, 9, 17-19, 22, 25, 33-35, 38, 41 and 49-52 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2002/0190215 (Tashiro). Applicant respectfully traverses this rejection.

Claims 1, 17 and 33 recite a pixel having "a circuit portion for supplying a reset signal and a photosensor charge accumulation signal to a column line; [and] a first storage circuit for receiving said reset signal from said column line and storing said reset signal, said first storage circuit comprising a first sample and hold transistor switchably coupling a first terminal of a first storage capacitor with said column line." Claims 1, 17 and 33 further recite "a second storage circuit for receiving said photosensor charge accumulation signal from said column line and storing said photosensor charge accumulation signal, said second storage circuit comprising a second sample and hold transistor switchably coupling a first terminal of a second storage capacitor with said column line."

Tashiro, in contrast to the claimed invention, refers in FIG. 10 (reproduced on the next page) to a circuit that supplies reset and photosensor charge accumulation signals directly to the two storage circuits (with storage capacitors CH1, CH2) by coupling the source follower transistor (M4) of the circuit to the sample transistors (M8, M11) of each storage circuit. The storage circuits in Tashiro then supply the reset and photosensor charge accumulation signals to the column line (coupled to source follower transistors M10, M13 of the storage circuits). *See* Tashiro at FIG. 10, para. 0091.

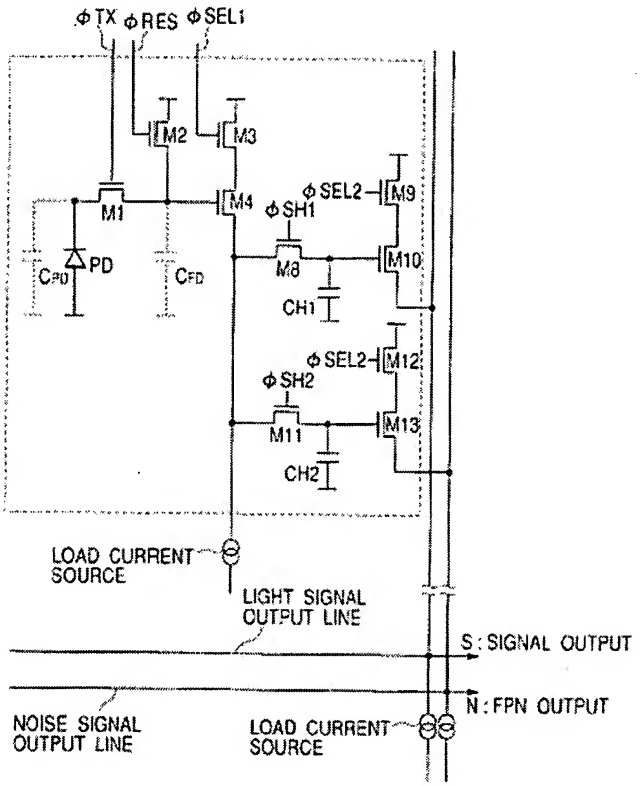

FIG. 10

In contrast, as recited by the claimed invention and shown in FIG. 2 (reproduced on the next page) of the present application, the claimed invention comprises a circuit portion that first supplies the "reset signal and [the] photosensor charge accumulation signal to a column line," and first and second storage circuits that receive the signals from the column line. This is different from the method and structure of Tashiro. Tashiro does not teach or suggest a circuit portion for supplying a reset signal and a photosensor charge accumulation signal first to a column line and then to two storage circuits switchably connected to the column line for storing the signals. Instead, in Tashiro, the circuit supplies the reset and photosensor charge accumulation signals directly to the two storage circuits. Using the configuration of the claimed invention, a reduction in kTC noise is achieved. Hence, Tashiro does not teach or suggest all limitations of claims 1, 17 or 33. Therefore, Tashiro fails to anticipate claims 1, 17 and 33. Claims 2-3, 6, 9, 18-19, 22, 25, 34-35, 38, 41 depend from claims 1, 17 and 33 and should be allowable along with claims 1, 17 and 33.

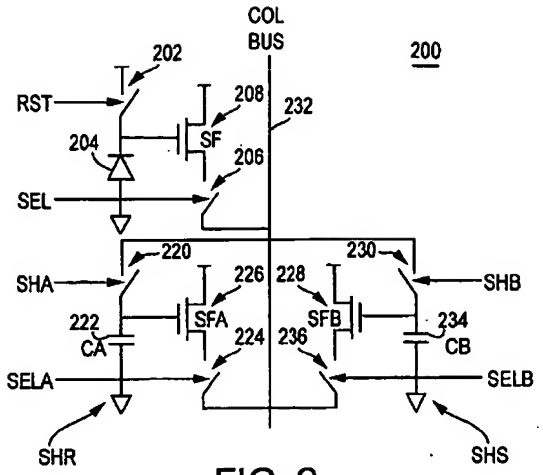

FIG. 2

Claim 49 recites a method comprising the step of "transferring a reset signal from the circuit portion to a column line [and] receiving the reset signal from the column line at the first storage circuit. Claim 49 also recites the step of "transferring a charge accumulation signal from the circuit portion to a column line [and] receiving the charge accumulation signal from the column line at the second storage circuit."

Tashiro, in contrast, teaches transferring reset and photosensor charge accumulation signals directly to the two storage circuits, which then supply the signals to the column line. *See* Tashiro FIG. 10, para. 0091. Tashiro does not teach "transferring [signals] from the circuit portion to a column line [and] receiving the [signals] from the column line at the [first or second] storage circuit." Hence, Tashiro does not teach or suggest all limitations of claim 49. Therefore, Tashiro fails to anticipate the claimed invention. Claim 50 depends from claim 49 and should be allowable along with claim 49.

Therefore, the rejection should be withdrawn and the claims allowed.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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